

# FDC655BN

## Single N-Channel, Logic Level, PowerTrench® MOSFET

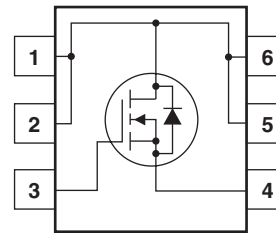
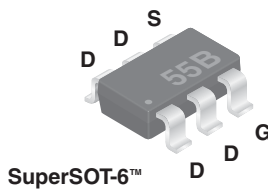
### Features

- 6.3 A, 30 V.  
 $R_{DS(ON)} = 25\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(ON)} = 33\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Fast switching
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(on)}$

### General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimized on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	6.3	A
		20	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6	W
		0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$
<b>Thermal Characteristics</b>			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C}/\text{W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.55B	FDC655BN	7"	8mm	3000 units

### Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		23		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = -55^\circ\text{C}$			1 10	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4.1		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}, T_J = 125^\circ\text{C}$		20 26 27	25 33 45	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 6.3\text{ A}$		20		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		570		pF
$C_{oss}$	Output Capacitance			140		pF
$C_{rss}$	Reverse Transfer Capacitance			70		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.1		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
$t_r$	Turn–On Rise Time			4	8	ns
$t_{d(off)}$	Turn–Off Delay Time			22	35	ns
$t_f$	Turn–Off Fall Time			3	6	ns
$Q_{g(TOT)}$	Total Gate Charge at $V_{gs}=10\text{V}$	$V_{DD} = 15\text{ V}, I_D = 6.3\text{ A},$		10	15	nC
$Q_{g(TOT)}$	Total Gate Charge at $V_{gs}=5\text{V}$			6	8	nC
$Q_{gs}$	Gate–Source Charge			1.7		nC
$Q_{gd}$	Gate–Drain Charge			2.1		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 6.3\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		18		ns
$Q_{rr}$	Diode Reverse Recovery Charge			9		nC

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.
  - $78^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2oz copper on FR-4 board.
  - $156^\circ\text{C}/\text{W}$  when mounted on a minimum pad.
- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

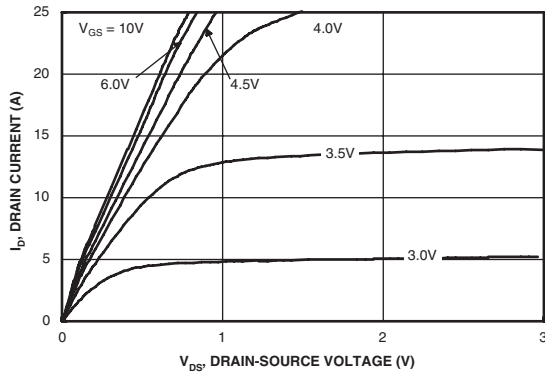


Figure 1. On-Region Characteristics.

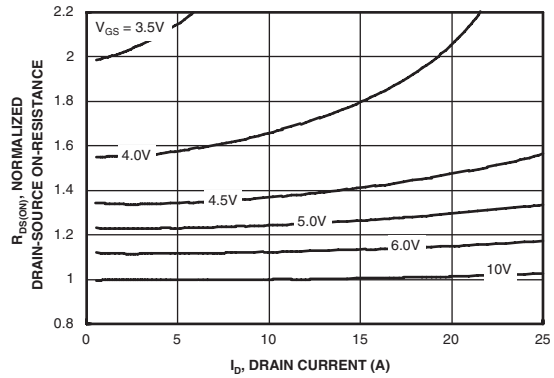


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

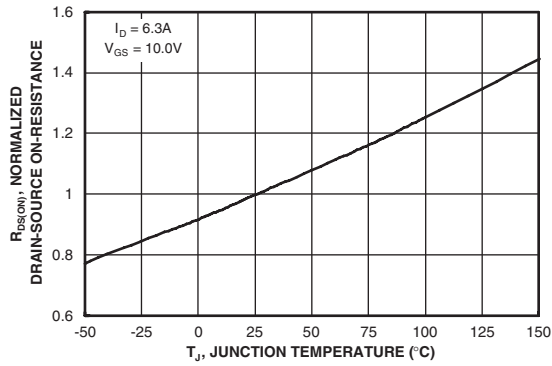


Figure 3. On-Resistance Variation with Temperature.

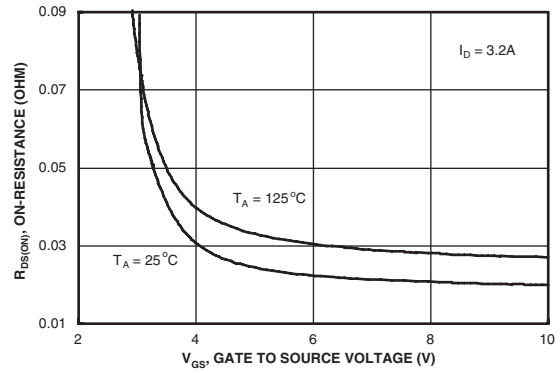


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

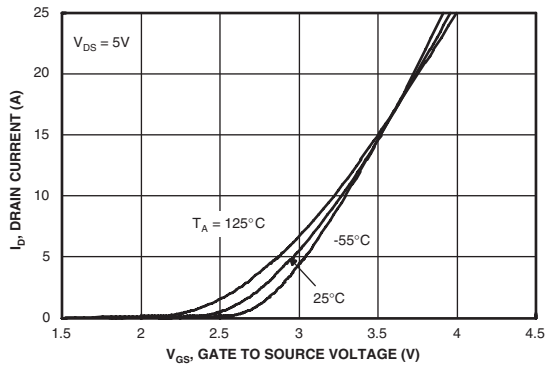


Figure 5. Transfer Characteristics.

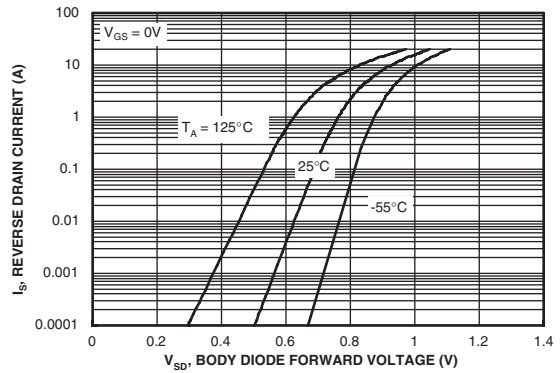


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

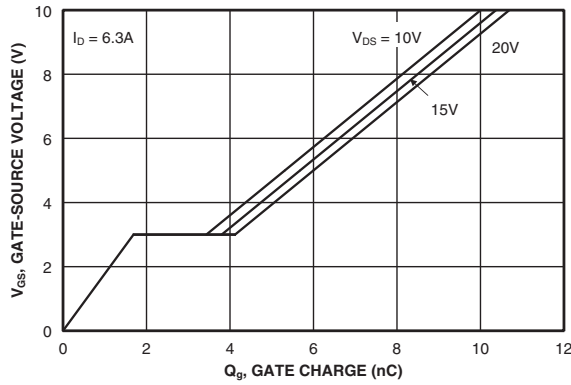


Figure 7. Gate Charge Characteristics.

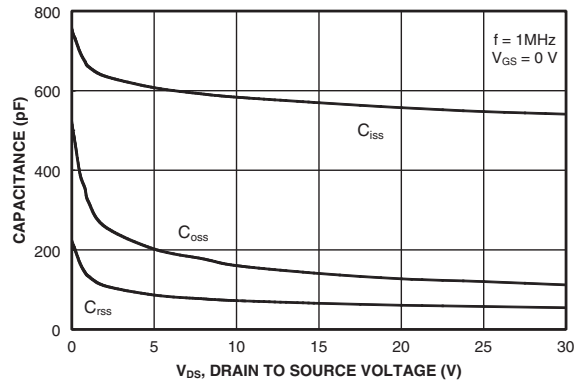


Figure 8. Capacitance Characteristics.

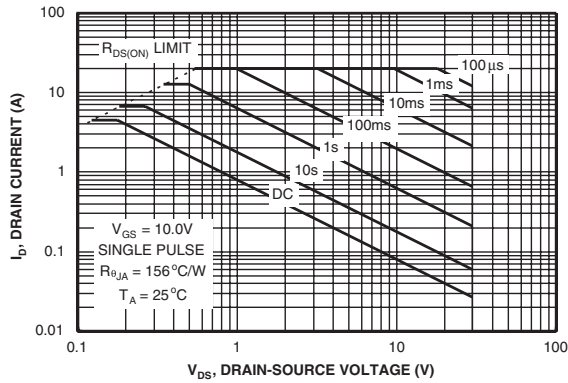


Figure 9. Maximum Safe Operating Area.

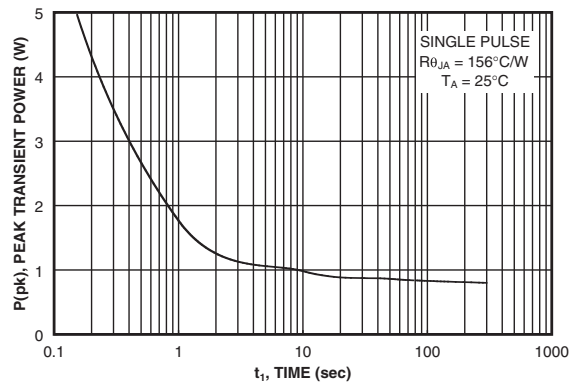


Figure 10. Single Pulse Maximum Power Dissipation.

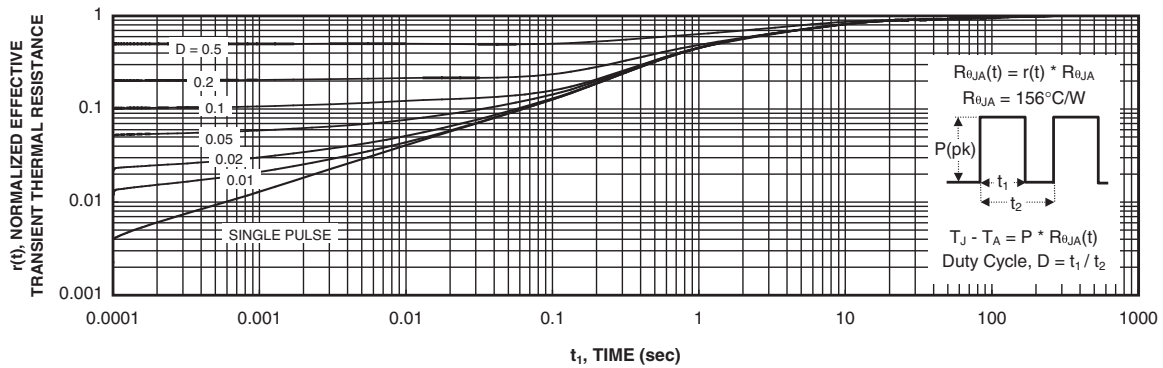
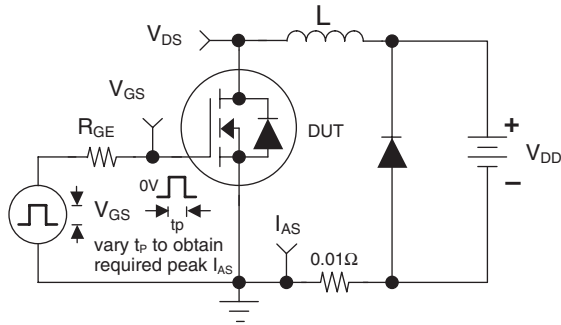


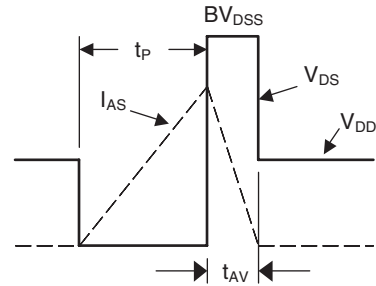
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

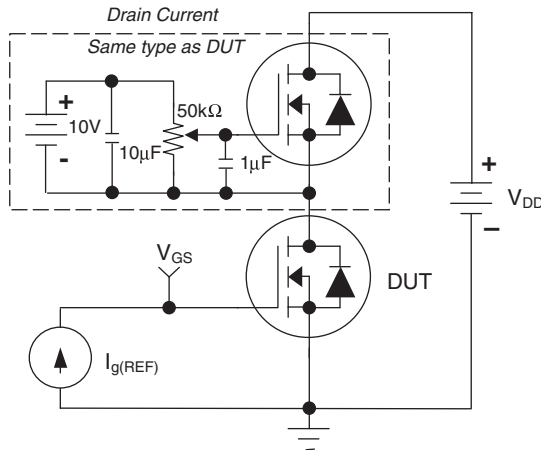
## Typical Characteristics



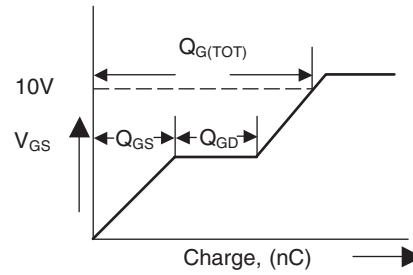
**Figure 12. Unclamped Inductive Load Test Circuit**



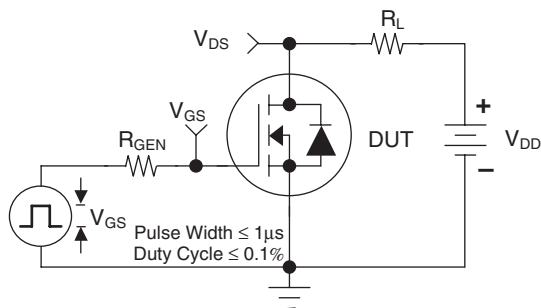
**Figure 13. Unclamped Inductive Waveforms**



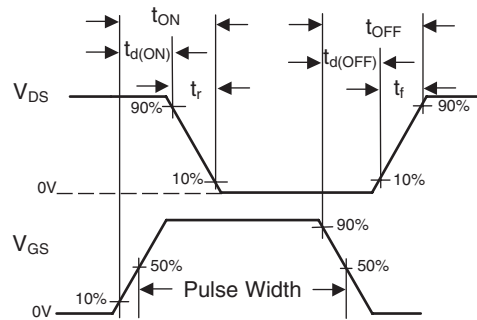
**Figure 14. Gate Charge Test Circuit**



**Figure 15. Gate Charge Waveform**



**Figure 16. Switching Time Test Circuit**



**Figure 17. Switching Time Waveforms**

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